IN THE CLAIMS

Please amend the claims as follows:

1. (Previously presented) A duty cycle correction circuit comprising:

a delay unit for receiving a first clock signal in which a first logic value has a shorter period of time per cycle than a second logic value, delaying the first clock signal, and outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value; and

a clock-signal output unit for outputting a third clock signal based on the first and second clock signals,

wherein the clock-signal output unit comprises: a first output unit for setting the third clock signal at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value; and a second output unit for setting the third clock signal at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal to the second logic value,

the delay unit includes a transfer gate which is put into condition to pass the first clock signal to output the second clock signal,

the transfer gate includes a transistor whose gate and drain are connected to each other, and

the duty cycle correction circuit receives the first clock signal and corrects the duty cycle of the first clock signal to output the third clock signal.

2-5. (Cancelled)

6. (Previously presented) The circuit of claim 1,

wherein the first clock signal is produced by a frequency divider circuit formed of at least one n-channel transistor and at least one p-channel transistor,

the clock-signal output unit is formed of at least one n-channel transistor and at least one p-channel transistor, and

the numbers of n-channel and p-channel transistors through which a signal travels in the rising of the third clock signal are equal to those through which a signal travels in the falling of the third clock signal.

7. (Cancelled)

8. (Currently amended) ~~The circuit of claim 7,~~ A 50% duty cycle clock-signal production circuit comprising:

a delay unit for receiving a first clock signal in which a first logic value has a shorter period of time per cycle than a second logic value, delaying the first clock signal and outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value;

a clock-signal output unit for outputting a third clock signal based on the first and second clock signals; and

a frequency divider circuit for producing the first clock signal,

wherein the clock-signal output unit comprises:

a first output unit for setting the third clock signal at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value; and

a second output unit for setting the third clock signal at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal to the second logic value;

wherein the delay unit includes a transistor whose gate is supplied with a predetermined voltage and of which either one of a source and a drain receives the first clock signal to output the second clock signal from the other of the drain and the source,

the predetermined voltage supplied to the gate of the transistor is above a gate threshold value in the case where the transistor is an n-channel transistor while the predetermined voltage supplied to the gate of the transistor is below the gate threshold value in the case where the transistor is a p-channel transistor,

~~wherein~~ the frequency divider circuit is formed of at least one n-channel transistor and at least one p-channel transistor,

the clock-signal output unit is formed of at least one n-channel transistor and at least one p-channel transistor, and

the numbers of n-channel and p-channel transistors through which a signal travels in the rising of the third clock signal are equal to those through which a signal travels in the falling of the third clock signal.